TED software tools for thermal evaluation of integrated circuits

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Abstract **- Although several types of design verification tools have been recently added to the IC design flow, adequate tools for thermal analysis during the design process still does not exist. In the absence of thermal analysis, not only can excessive hot spots affect reliability but important differences between expected and actual performances may compromise circuit functionality. We have introduced a new physical design verification tool TED, integrating thermal analysis into the design flow. Starting from extracted view this tool automatically verifies for each device its temperature and power density, checks whether maximum ratings are not exceeded. It yields circuit simulation accounting for realistic temperature distribution without modifying device models.**

1 Introduction

Increasing component density, operation speed, and new high current technologies results in elevated device temperatures and high temperature gradients between the devices in different locations on the same integrated circuit. Electrical performances of the devices are temperature dependent. Heat generation in devices produces thermal responses that alter electrical performance. This coupled electrical-thermal behavior, if not addressed during circuit simulation, may lead to performance degradation, thermal instabilities, and thermal failure if insufficient cooling is provided.

The importance of these effects is much larger than only reliability issues, including device mismatch, temperature dependent delays on the signal path or level mismatch affecting noise margins. Therefore, during the design of integrated circuits, it is important to predict the electrical performance accounting for the thermal response. From the reliability point of view, it is important to ensure that none of the hot spots exceeds maximum admissible device temperature. However several approaches to resolve this problem were proposed, a global and calculus efficient solution is still lacking. The only global solution proposed [Szek97] [Szek99] [Szek00] is based on simultaneous iteration of concatenated electric and thermal equations, modifies device models and uses FFT based thermal simulator.

With TED software toll set Pultronics has developed a global methodology and tools for performing coupled electro-thermal analysis of IC devices in an efficient and fully automated manner, i.e. directly from the design framework, extracting circuit geometry from the layout, using commercial circuit simulator, without modifying foundry supplied device models and using fast thermal algorithms. TED provides a global practical solution to electro-thermal IC analysis and enable a practical application of the method. TED provides a platform for a layout based electro-thermal simulation directly plugged in the design platform. Hence, problems associated with thermal performance degradation, thermal coupling of devices, and thermal instabilities may be predicted during the device design and corrected to preclude such problems after fabtication.

2 Introduction

2.1 High temperature gradient on the die surface

As mainstream circuit and system design heads towards deep submicron, the power management and related to it thermal analysis, both integrated in a design environment, become essential. With the increasing component count and density of integrated circuits, continuing development of systems-on-chip (SOC) and increasing data rate, the power dissipation from the single circuit dramatically increased over the last few years. This tendency is illustrated by the power dissipation of recent high-performance microprocessors, Table 2.1.1 , with the heat flux exceeding 10 W/cm^2.

Microprocessor	Technology	Devices	Power [W]	Size [mm2]	Heat Flux [W/cm^2]
DEC 21264	0.35m CMOS	15,200,000	72	302	23.84
Intel Pentium Pro	0.35µm BiCMOS	5,500,000	30	195	15.30
UltraSPARC II	0.35m CMOS	5,400,000	25	149	16.77
Exponential X-704	0.5µm BiCMOS	2,700,000	85	150	56.67
F-RISC/G [ ]	GaAs HBTs	301642	220	2101	10.47

Table 2.1.1 Power dissipation of recent high-performance microprocessors

High power density results in the increased operation temperature of the circuit and usually in local hot spots. High power consumption in the dense regions subjected to a high switching activity like ALU or cache blocks leads to non-uniform heat flux and temperature distribution on the block level. This non-uniformity is even more pronounced on the device level. The area occupied by the devices, and more precisely their active area where power is dissipated, is

very small compared to the total die area, as shown in Table 2.1.2. The heat flux on the surface of the chip is thus highly non-uniform.

Chip Name	Total Devices	Total Area [mm2]	Device Area	Wire Area	Metal Layers
Cache RAM []	14300	64.4	4.4%	95.6%	3
Pentium Pro* (0.35 µm)	5,500,000	195	7.25%	92.25%	

*CMOS (device area approximated by 21 x [minimum design rule].

Table 2.1.2 Comparison of interconnect area and device area.

Taking in consideration very small features of dissipating devices, power dissipation is mainly limited to the active channel or base area, and limited thermal conductivity of semiconductor (2.2 [W/^{o}Cin] for Si and 0.76 [W/^{o}Cin] for GaAs), the temperature distribution on the surface may be very non-uniform. Very high hot spots reaching several tens Celsius degrees over substrate temperature where already reported for GaAs FETs , AlGaAs or GaInP based HBT circuits [Smit86] [Smit91] [Anho95] [Wald92] [Greg97]. It is characteristic for GaAs based substrates, having much lower thermal conductivity than silicon, that hot-spots are abrupt and most of the temperature drop is localized within few µm from the dissipating area. For a CMOS process (0.5µm) a spatial temperature differences as high as 20.65°C on a 2x2mm chip were reported [Chen00]. This research stress that even for CMOS process temperature distribution has to be considered.

High temperature gradient on the die impacts a standard IC design flow assuming that all the devices are in the same temperature This temperature used as a global parameter depended only on the mean power dissipation of the chip, thermal conductivity of the materials (die, package, PCB) and ambient temperature. Temperature was considered mainly as a “corner” parameter to ensure a correct operation of the circuit.

If temperature estimation is based on the assumption of uniform heat flux from the surface, also known as the parallel plate case [Poul91], it can lead to an over-optimistic result. It may definitely compromise circuit reliability. But what is very important from the designer point of view, performance of particular devices may vary independently, altering or compromising circuit performance.

An example of temperature dependent deviation of performances is given with the description of the applied algorithms.

3 Previous work

3.1 Thermal modeling

The objective of thermal modeling process is to create a model which represents the thermal behavior of the physical system. The thermal modeling process requires material parameters, structure geometry and power dissipation pattern to formulate the heat equation. The geometry can be extracted from a layout. In the case of integrated circuits the physical system can be approximated by several small tetrahedral sources, often characterized by a high aspect ratio, are immerged in a semi infinite plate of semiconductor substrate. Power dissipation pattern is given by power dissipation of individual devices. Once differential equations representing heat transfer within given boundary conditions are formulated, they have to be solved by thermal simulator.

A large variety of approaches dedicated to thermal modeling can be found in literature, . There are several methods to solve heat equations: finite difference [Dige96], finite element [Wuns97], [Chu95], boundary element approaches [Sabr97], [Dris90], Fourier series [Szek96], analytical solutions [Poul92]. Most of the approaches to formulate the problem for integrated circuits are valid only in steady state and for linear equations. The temperature dependent thermal conductivity of semiconductor material, which is characteristic for GaAs substrate, leads to a nonlinear heat equation and has to be considered in the modeling process

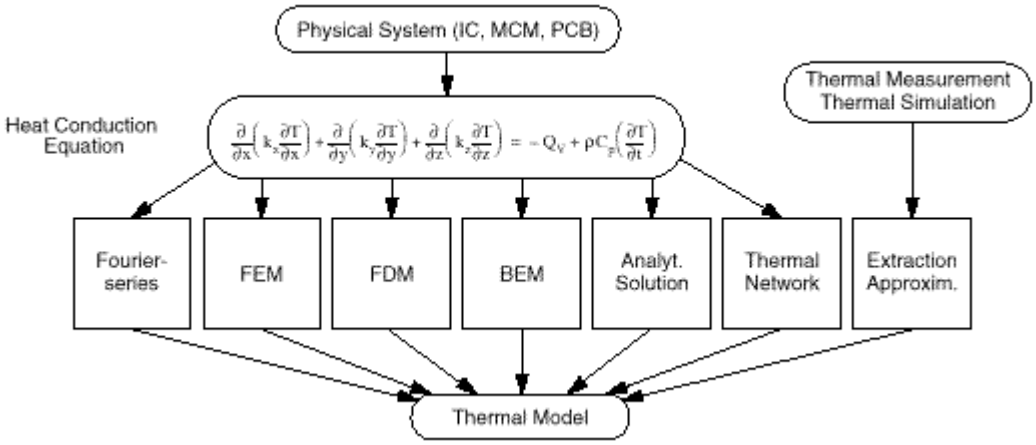


Figure 3.1.1 Basic approaches for thermal modeling [Wuns97]

The most commonly used finite–element (FEM) method divide the investigated 3D structure into small volumes. Simulator approximates the heat transfer

equation for each volume by a linear or quadratic equation and solves the linear set. The concept and application of FDM is similar, essentially the volume is discretized, thermal resistances between neighboring elements are calculated and a network is solved.

The great advantage of FEM or FDM is their generality. However taking a very specific geometry of integrated circuits, specifically very small and flat power sources, the reasonable mesh is becoming very complex already with few devices. This results in very lengthy simulation times, and becomes practically impossible for larger circuits.

Another class of thermal simulators uses Fourier expansion to solve heat equations, however is suited only for a limited set of boundary conditions.

Direct solution to Poisson equation was first proposed by [Smit86], [Smith91], and was used by several other groups [Lee93], [Veijo97]…

3.2 Electro-thermal simulation

During the last five years, the intensified activities in the field of thermal modeling of integrated circuits and electro-thermal simulation were observed. There are two principle approaches the direct method and relaxation method, as shown in Figure 3.2.1.

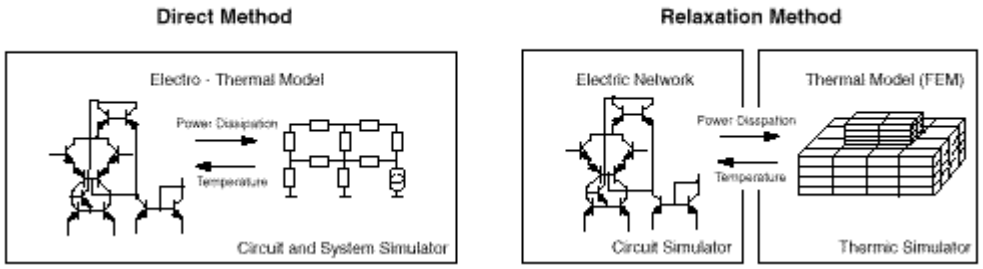


Figure 3.2.1 Direct and relaxation approaches for thermal simulation [Wuns97]

The relaxation method is based on coupling two independent simulators, thermal and circuit simulators [Wuns97]. To solve the electrical and thermal equations, two separate representation of the circuit are created, one purelly thermal and one electrical. Two separate specialized solvers are used. Each simulator uses the updated information from other simulator in an iteration loop. In general, the modeling process for the relaxation method is straight forward however it is

necessary to provide means to realize data transfer, synchronization and convergence control.

On the contrary to the relaxation method, the direct method, known also as simultaneous simulation, is based on modeling of the thermal and electronic behavior of the circuit for a single simulation tool [Szek96], [Szek99]. Thermal behavior of any dissipating source can be modeled by similar equations as the equations solved by electrical simulators. It can be therefor described by same analog behavioral language. Thus each dissipating device has to be substituted by an electro-thermal device as symbolically depicted in Figure 3.2.2. The instantaneous dissipation is forced to the thermal node as a current. The device function depends on the temperature (voltage) data of this node. Thermal interactions between devices are represented by a thermal network.

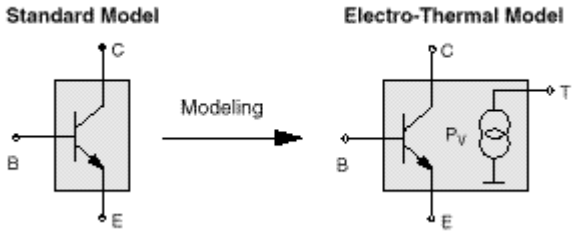


Figure 3.2.2 Symbolic representation of electro-thermal device model [Wuns97]

For the direct method one global netlist containing both electrical and thermal information is generated. Thus same circuit simulator in a single run will solve both sets of equations, electrical and thermal. A standard commercial circuit simulator processes the simulation. However it has to be stressed that thermal network should be already known prior to the simulation. Thus thermal models for all interacting devices has to be calculated anyway. To describe simultaneous method the methodology used by [Szek99] will be discussed, as this is the most advanced implementation to date.

In simultaneous iteration the iterative solution takes place simultaneously for the thermal and electrical sub-network, resulting in a possibility of observation transients, which is the major advantage of the direct method. The main drawback results from its complexity on several levels. The device models have to be electro-thermal, having a thermal node besides the electrical nodes, which is an important modification of foundry models.

At the same time, the thermal model of the structure has to be defined. The complete thermal system is represented by a thermal N-port, as depicted symbolically in Figure 3.2.3 for a two-transistor circuit. The thermal N-port can be described as a set of functions relating the dissipation vector P of the system to its temperature vector T:

$T_i = f_i(P_j)$,
where i, j=1,…N, and T_i is a temperature of i-th node, P_j is a power excitation of j-th node.

The complexity of such a system in N^2. The additional functions are needed to model heat transfer to ambient.

Each of this functions is approximated by a K element RC ladder, where K is about 10-16, as depicted on Figure 3.2.3. The resistance matrix alone describes a steady-state case. The capacitors are added to model a dynamic behavior of thermal system. A set of such thermal RC ladders is used to describe the in-chip thermal couplings and the device-to-ambient couplings, what furthermore complexifies the system to be solved.

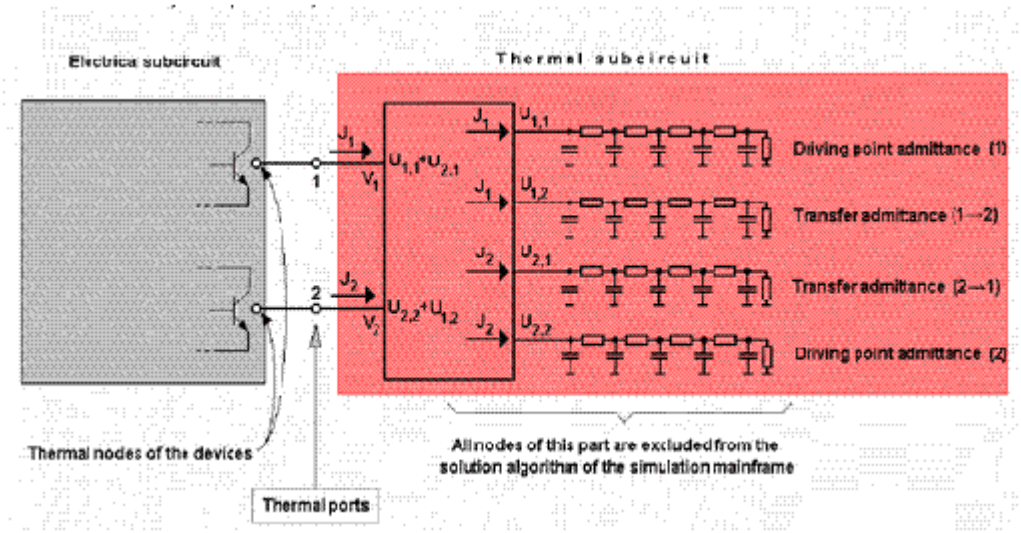


Figure 3.2.3 Model of a coupled electro-thermal network used in [Szek99]

All the functions *fi* has to be calculated. To calculate them a special engine was conceived executing a following algorithm.

(a) thermal solver is used for thermal characterization of the physical structure. A series of 3-D dynamic thermal simulations has to be run (THERMANAL [Szek99]). Each time one dissipating element is selected and a thermal excitation is applied to it. The thermal response of all other elements, each at a time, is calculated and recorded. This operation is repeated few times for each element.

(b) thermal model generator is used to calculate compact model for thermal interactions within the structure. An algorithm was created (THERMOMODEL [Szek99]) to calculate RC ladders for each pair of

devices, based on the collected data. Solutions for each *fi* function can be calculated separately,

Once thermal models were calculated for each element in the thermal network (set of thermal RC ladders) is added to electric netlist and processed by the circuit solver. If a thermal map has to be produced afterwards, the power dissipation data has to be processed once more by thermal solver. For each point, a superposition of thermal influences from each device has to be calculated.

The precision of the final solution, for this strategy, depend not only on the thermal simulation itself, which is sufficiently precise, but on the thermal network RC model. This set of RC ladder models has to fully describe the thermal environment of the circuit. Since in realistic case there exists a thermal relation between any two nodes of the circuit, than thermal model becomes huge for a relatively small circuit. There is a clear trade-off between the size of thermal network and precision of the model. The thermal network has to be compact enough to provide a reasonably fast solution when linked to the electrical solver. The authors suggest themselves that compact models are needed.

Other characteristic, that can be observed, is that this method does not allow to account for a temperature dependent thermal conductivity.

Major advantages and disadvantages of both methods may be summarized as follows.

Direct method

- Advantages
  - Capable to model thermal transient behavior
- Disadvantages
  - huge number of nodes for circuit solver, dramatically increasing simulation times; more compact thermal models needed.
  - processing time necessary to build thermal network;
    For each dissipating device in the network a dedicated set of thermal simulation is needed. This data has to be processed to calculate an approximate RC model for each pair of devices. This is an extremmaly lenghy process. For a 64 element system the generation of equivalent thermal model takes 100min on a Sun Sparc20 station. A 64 element circuit usually represent only a small block in an integrated system
  - As the direct consequence of this approach becomes prohibitively slow for large systems
  - Unable to handle temperature dependent thermal conductivity of the substrate

- Industry standard SPICE versions (HSPICE, PSPICE) do not support real electro-thermal models
- Leading SPICE MOS models (e.g.BSIM3) are not real electro-thermal models

Simulator coupling

- Advantages
  - Calculus efficient
  - Does not require extraction of simplified thermal models
  - Does not alternate foundry models
  - Potentially capable of handling a temperature dependent thermal conductivity. This actually depends on the thermal solver
  - The size of designs the simulator is capable of handling depends on the capabilities on both simulators separately. Mainly it can handle large designs if thermal simulator can
- Disadvantages
  - Difficulty in handling transients

    However it was shown [Wuns97] that electro-thermal transient analysis with simulator coupling is possible.

3.3 Integration into design framework

To enable practical application of the electro-thermal analysis of integrated circuits, the global solution providing an automated transfer of data between simulators and access to the design database was necessary. The first integration of electro-thermal simulation with a design database was proposed by [Szek97] and evolved until recently [Szek99]. The flow chart illustrating this methodology is depicted in Figure 3.3.1. An important change between versions is that in the earlier one two separate extracted views were generated. Once the layout of the circuit and the extraction are done the netlister generates two separate netlists, one for thermal simulator and the other for electric circuit simulator. The thermal solver proceeds with modeling of the thermal interactions between any chosen pair of devices, and thermal model generator extracts corresponding models. Both netlists are then concatenated, solved and processed once more by thermal solver to calculate the thermal map.

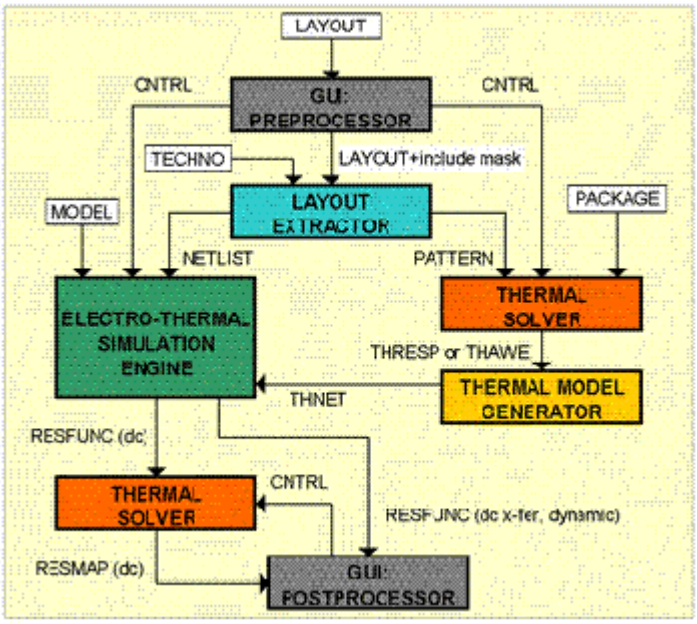


Figure 3.3.1 Flowchart following ref [Szek99]

3.4 Temperature sensors

Numerous solutions for CMOS compatible temperature sensors for thermal testing purposes have been developed by various groups in the past years. For thermal monitoring purposes and for performing the sensing function in built-in thermal test circuitry a compact, low power sensors are most suitable

The best suitable for on-chip sensing seems the current reference based sensors as e.g. [Szek98], with a current- frequency converter. The I output current decreases as the temperature increases. This operation is based both on the temperature dependence of the threshold voltage and the carrier mobility. The right hand side of the circuit is a current-to-frequency converter, providing a square wave as output signal, the frequency of which is directly related to the temperature.

4 TED tool set - advantages of global approach

TED tool set resolved the paradigm of the electro-thermal analysis of integrated circuits using described below methodology. This methodology aims a post-layout analysis of the circuits and may be used by designers to more accurately model circuits, to help optimize circuits without over-designing them, or to detect thermal problems of the circuit before fabrication.

These algorithms enable to account for a realistic temperature distribution on a chip during the design process, thus generating thermally correct simulations. Designs may thus be more effectively validated prior to manufacturing, avoiding the risks of repeated prototyping or reliability problems. In consequence, development time and time-to-market are shortened while production yield and circuit reliability are increased. The circuit life-expectancy rapidly decreases with raising temperature. The failure rate doubles approximately every 10^{o}C. Local agglomeration of dissipating devices causes a very steep local temperature rise. Local hot spots can be several degrees above surrounding substrate temperature. This situation will directly lead to defectuosities occurring in such areas during the circuit life cycle. This methodology will help to optimize circuit architecture and layout, decreasing the peak temperature in the hot spots and thus increasing the overall reliability of a circuit.

4.1 Algorithms

The used algorithms enable an efficient electro-thermal evaluation of the circuits. To be efficient the analysis have to be accessible directly from the design framework, has to use fast and sufficiently precise algorithms, has to be able to handle large design with sufficient precision, and within a reasonable time. Thus TED tool set implements:

- Electro-thermal simulation through simulator coupling (much smaller circuit to be simulated, faster simulation time, however few iterations possible)
- Analytical solution of Poisson equation chosen for thermal simulator (fastest from the discussed methods, and sufficiently precise)
- One extraction for both electric and thermal simulations
- One initial netlist for both electric and thermal simulations
- electro-thermal algorithm has a direct access to the design.

Thus the following structure of the tools are used for the electro-thermal simulation, as depicted in Figure 4.1.1.

The post prosessing algorithm, the thermal mapping tool, can be used for fast verification of the temperature and power density of each device, and to estimate thermal implications of devices placement. For fast visual evaluation, the isothermal map superposed on a circuit layout, Figure 4.1.2, to graphically would be very helpful. An option is offered to display the regions within a given temperature range or the regions exceeding a user-defined temperature value. This function lets rapidly identify the components whose junction temperature or power density exceed a desired value.

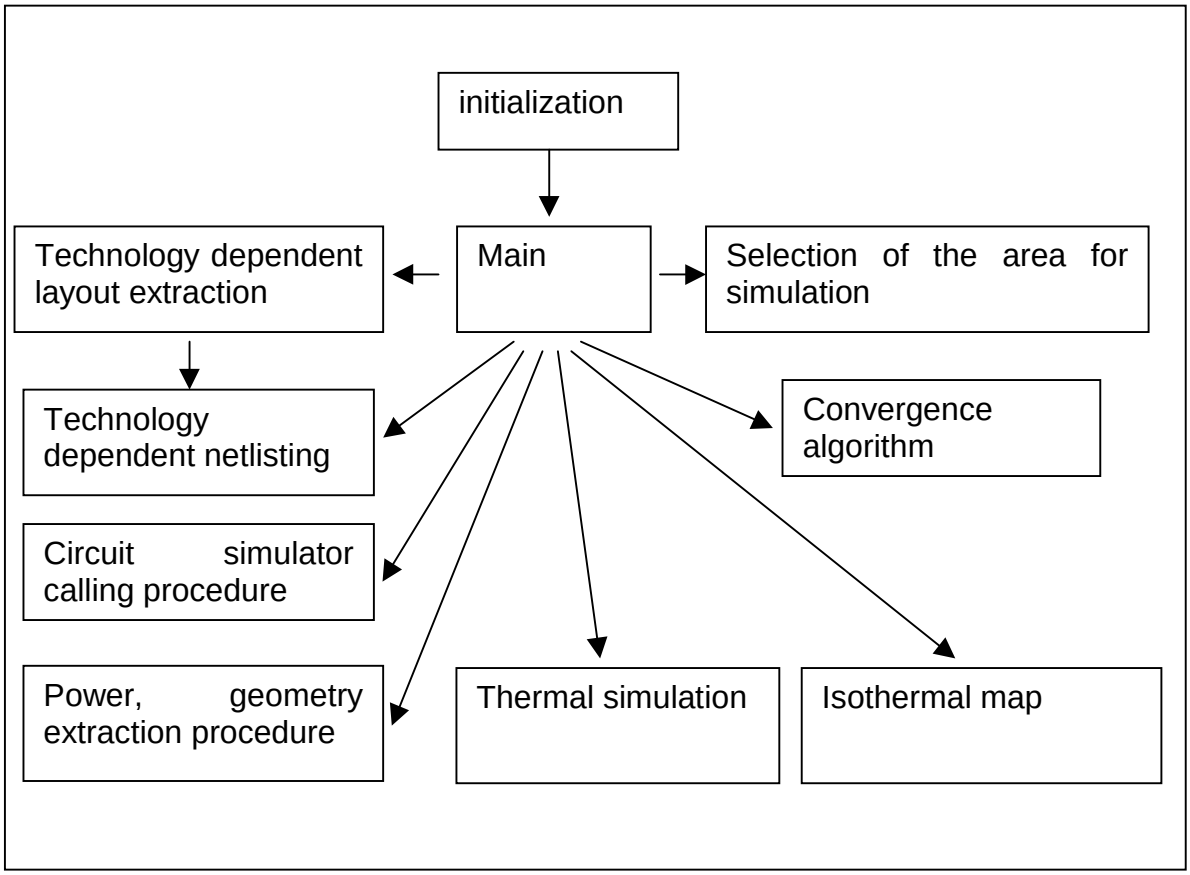


Figure 4.1.1 Proposed global flow-chart.

Since the electro-thermal analysis yields realistic device temperatures and it is the moment to verify whether any device do not exceed its maximum ratings (e.g maximum gate or drain current densities, maximum drain-source voltage, etc.), we have added a tool verifying it automatically. This analysis is effectuated during dc or transient simulations. To facilitate documentation the final implementation TED tool creates report file containing for each device its temperature, power density, and percentage of maximum ratings.

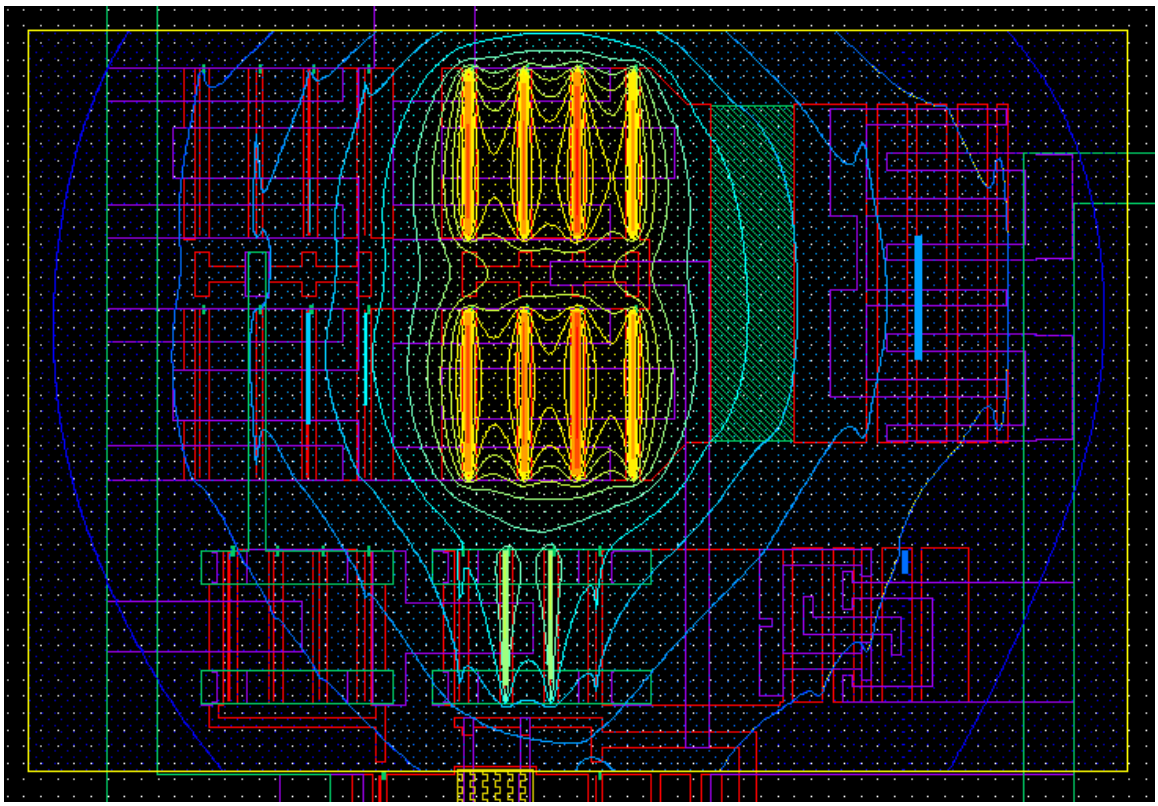


Figure 4.1.2 Example of a temperature distribution in an operational amplifier

Summarized capabilities:

- *thermally updated simulations* of the circuit performances including automatic extraction of circuit properties.
- *thermal map* of a circuit (superposed on a layout) enhanced with *hot spot detection and minimization*.
- *verification of percentage of maximum rating* for each device
- *import and analysis of the measured thermal signature of the DUT* (captured using liquid crystals or infrared camera), as a powerful tool for the test of prototype circuit.

4.2 Global flowchart

The algorithm access design databases and technology files within the design environment (implementation for Cadence ™) environment. The “extracted” view

and circuit netlist created and enhanced with all the geometrical and material information necessary for thermal mapping.

The electro-thermal simulator coupling loop is depicted in the flowchart of Figure 4.2.1. Device temperature depends on the dissipated power of all surrounding devices, and the device characteristics depend on the device temperature. The algorithm thus calls successively the electrical circuit solver (e.g. HSPICE) to extract dissipated power for each device and pass the data to the thermal algorithm to calculate temperature distribution on the die. The simulation stops if the variation of the temperature distribution between consecutive iterations differs by less than the user defined ΔT or if the number of iterations reach a user defined maximal value.

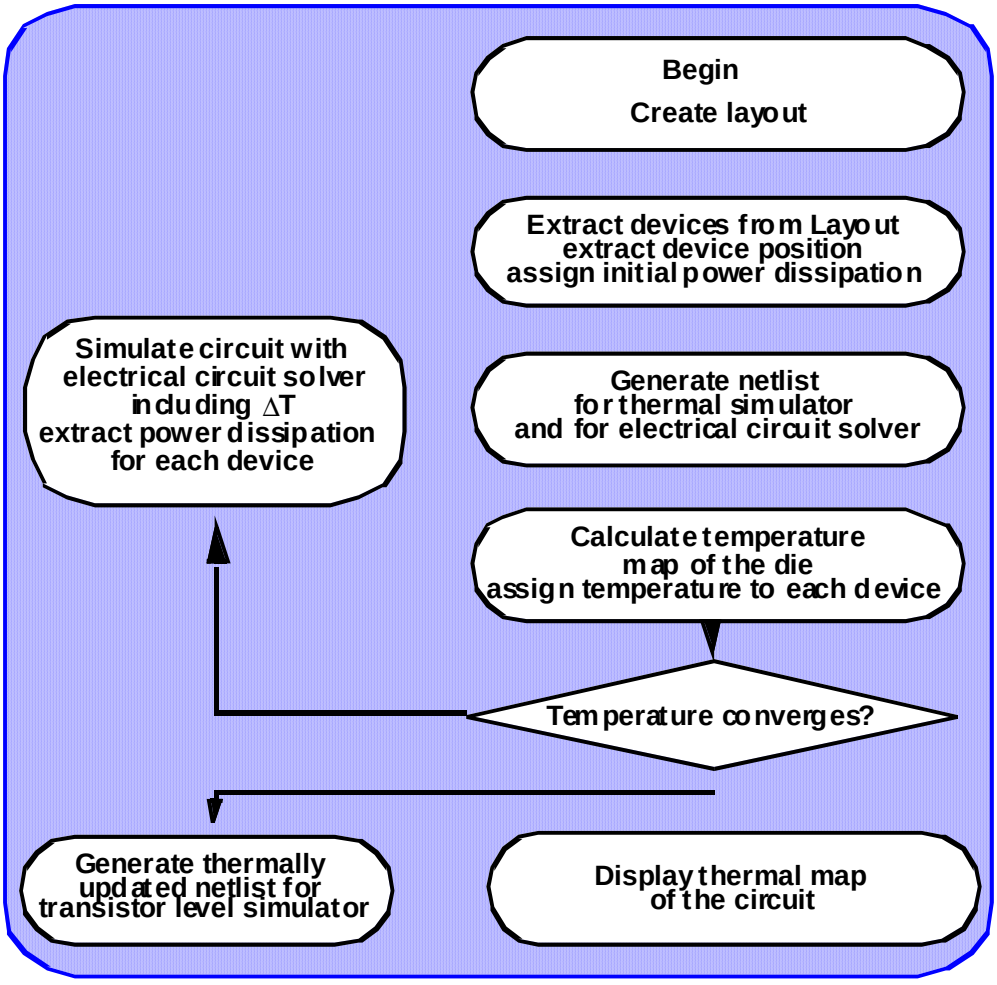


Figure 4.2.1 Flowchart Simulation coupling algorithm.

The thermal time constants associated with time-domain response to a power dissipation steps are very long. It was shown [Veji96] that for 4 finger GaAs

MESFET with w=2μm, l=100μm and gate separation of 25μm, a time constant associated with 1W power step is about 1ms. For high data rate or high frequency circuits a steady state approach to thermal analysis seems the most appropriate. In this case RMS values of power extracted from transient analysis are used to calculate a temperature map of a circuit.

Thermal analysis may be effectuated for steady state operation or for transient analysis by considering RMS power values over a chosen time period. The presented here algorithms provide very fast 2D map calculation with the flexibility to use automatic adaptive mesh generation.

The calculated thermal map may be displayed on the circuit layout. The peak temperature and power density for each device are reported in a file.

Algorithm used for thermal modeling

Temperature distribution on the die surface and more precisely on the cross-section through the middle of thickness of the dissipating area is calculated using a very computationally efficient method. This algorithm takes into account a set of simple geometries needed to represent the thermal structure of the IC.

The thermal model of an integrated circuit is geometrically represented as a parallelepiped filled with non-uniform materials, including metal and bulky heat sources. The modeling problem is simplified by assuming a uniform substrate, thus not accounting for the complex die structure. A separate very simple algorithm may be added to model the package and thus to estimate the substrate temperature. Second simplification is a substitution of bulky sources with flat uniform heat sources. To account for a high aspect ratio of the devices, the large devices are subdivided into smaller square devices. Both assumptions are generally sufficiently accurate and it was shown [Smit86], [Lee93] that this approach is adequate for IC modeling.

This algorithm solves the Poisson equation (0.1) with the temperature dependent thermal conductivity *k* and uses superposition to account for multiple heat sorces.

$$\nabla \cdot (k \cdot \nabla T) = q \qquad (0.1)$$

where *T(x, y, z)* is the temperature and *q(x, y, z)* is the power dissipation per volume unit. The thermal conductivity is temperature dependent and generally expressed as:

$$k(T) = k(T_0)\left(\frac{T}{T_0}\right)^n \qquad (0.2)$$

where *n* is typically -1.25 for both most popular semiconductor substrates GaAs and silicon.

To simplify the problem of the temperature dependent *k*, the algorithm calculates a pseudo-themperature rise τ expressed as:

$$\tau = T_0 + k^{-1}(T_0)\int_{T_0}^{T} k(T')\,dT' \qquad (0.3)$$

The inverse Kirchoff's transformation is then used to compute the real temperature rise T.

$$\Delta T = T_0\left[\left(\frac{(n+1)(\Delta\tau + T_0)}{T_0} - n\right)^{\frac{1}{n+1}} - 1\right] \qquad (0.4)$$

Several other algorithms were merged to this one to enhance precision (mirror image to model non-conducting die walls, []), or to accelerate calculus time (grouping distant elements to account for their influence as from one large element).

Comparing against 3-D FEM simulations

The results obtained using the described above algorithm were compared against the results obtained using 3-D Finite Element Based software package FlexPDE. FlexPDE is a software tool obtaining numerical solutions to the coupled sets of partial linear or non-linear differential equations. It uses a Galerkin finite element model, with quadratic or cubic basis functions involving nodal values of system variables only.

First we have considered one, than two closely spaced (30μm) Gallium Arsenide transistors (DFET, w= 50μm, l=0.6μm), each with a high power dissipation of 50mW in the channel area. Considered model consisted of GaAs 400x400 μm section of a 1000 μm thick wafer (twice standard wafer thickness). Bottom

contact was forcing 50 degC temperature, other boundaries were defined as natural (no heat flux through the boundary). What can be observed from the figures Figure 4.2.3 is that most of the temperature drop is local, very close to the device. In this example a 90% of temperature drop was observed within first 35 μm. The spatial distribution of the heat sources on the surface affects only the small depth of the substrate. Due to the algorithm complexity, more complex arrangements has to be analyzed as a superposition of influence of distinct sources, or as a periodic structures.

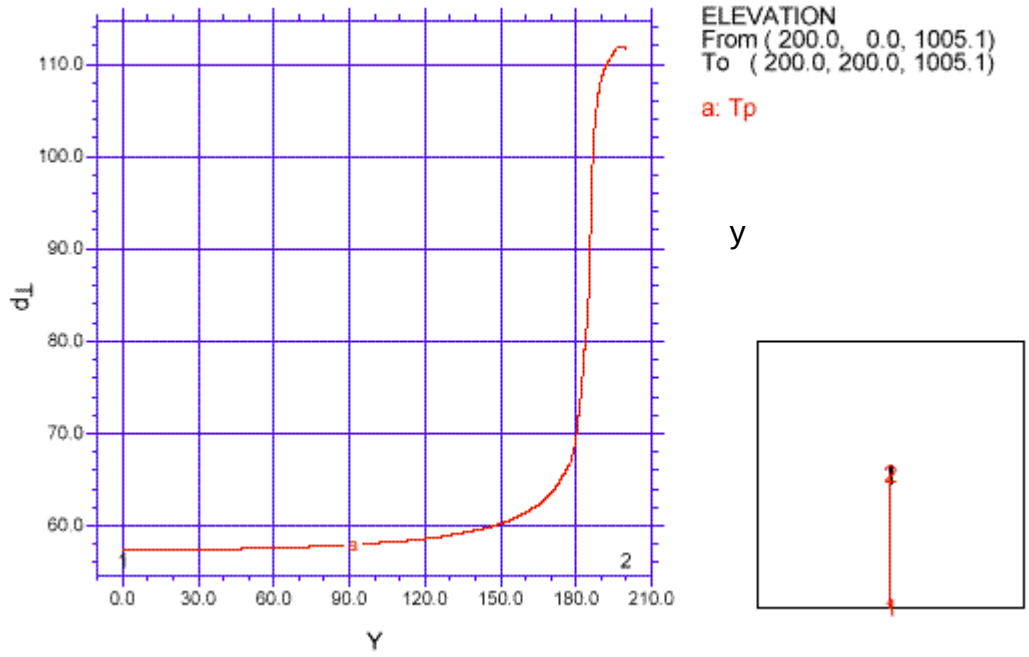
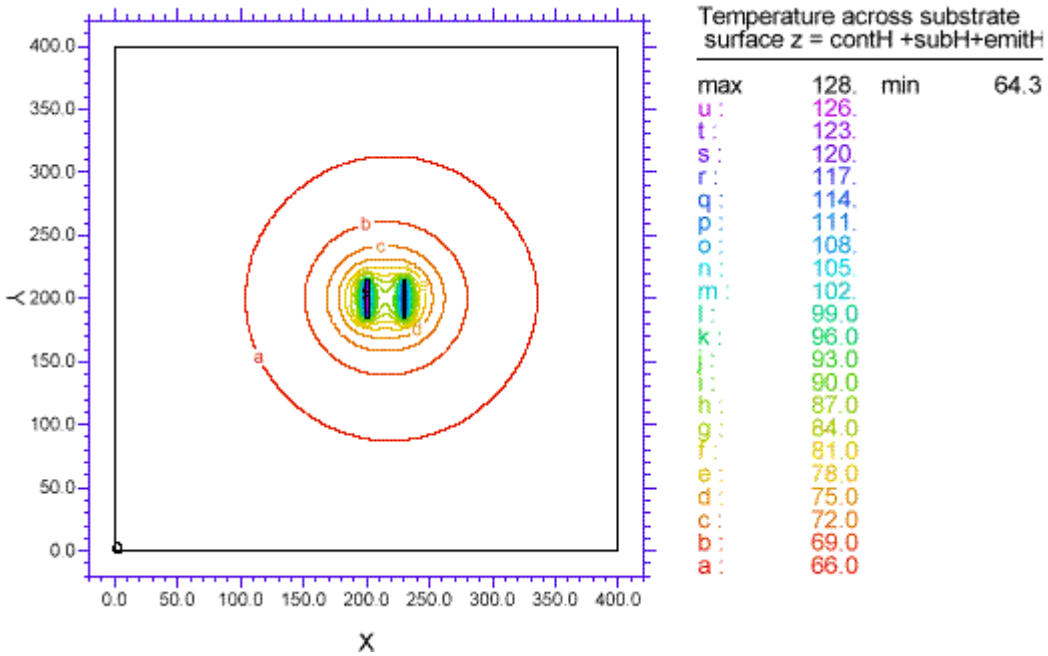
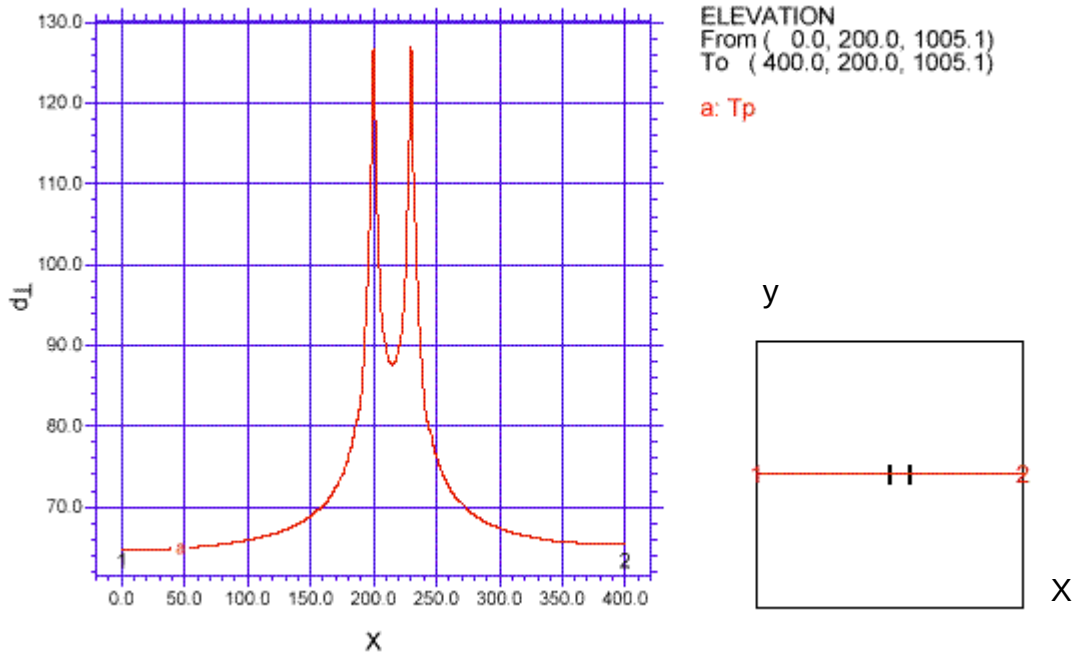


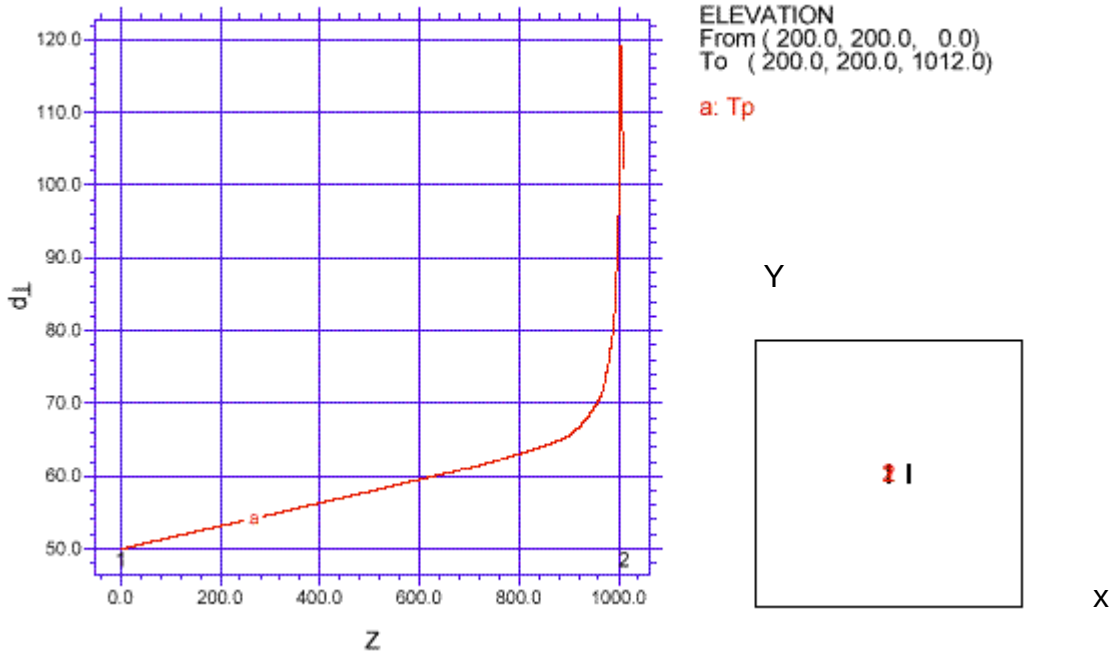
Figure 4.2.2 Temperature profile (Tp) due to a single device; XY device plane



(a) Temperature profile on the device plane: cross section at half of channel thickness



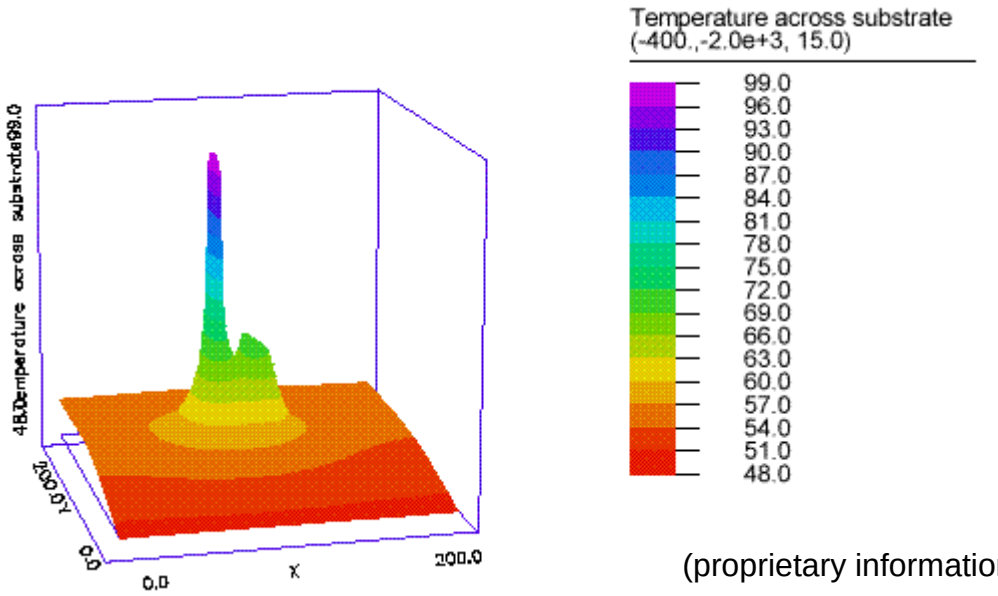
(b) Temperature profile on the device plane; temperature variation with the distance from the devices



(c) Temperature profile in the direction of the bottom contact

Figure 4.2.3 Temperature profiles in the case of 2 devices placed in YX plane

For the above simulations only the semiconductor layer was considered. Next the interconnect metal was added. In the considered example, first layer metal has a contact very close to the dissipating area. Other end of the metal line has an ohmic contact to the semiconductor relatively close to the device. Although the device dissipates the same 50mW, the main temperature peak is much lower and a second peak appeared, since this metal actively participated in the heat evacuation from the active area.



(proprietary information)

Figure 4.2.4 Temperature distribution in the device plane for a single transistor with interconnect metal

Based on this result, it is evident that a model of metal interconnects has to be added to the thermal modeling algorithm used for electro-thermal simulation, as it was implemented to TED tool set.

The developed tool set yields a high precision simulation results. For example the following figure illustrates the test results for a single device benchmark. The first figure shows test results for the original device having massive metal interconnects. The second figure presents the results obtained using equivalent Pultronics model and methodology. In this case metal interconnect evacuates about 50% of total dissipated power. Both results match within few percent.

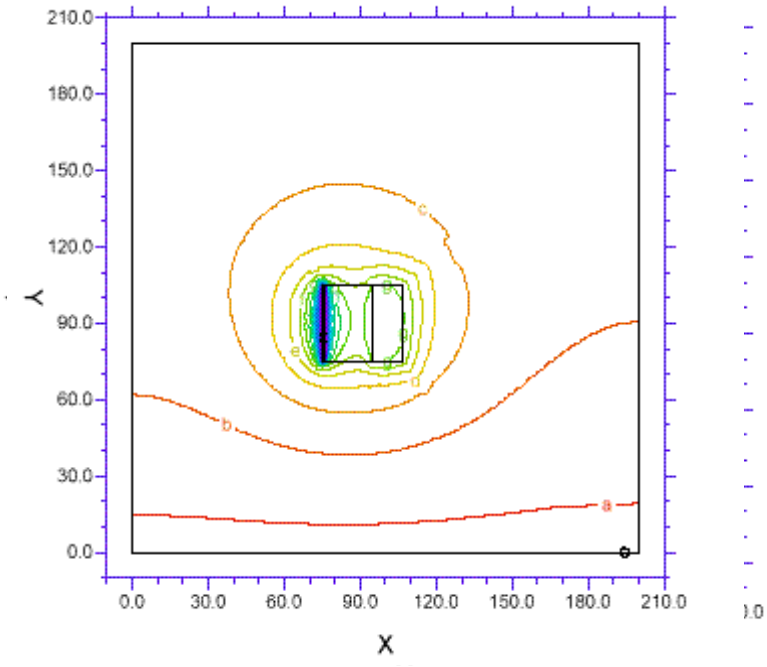
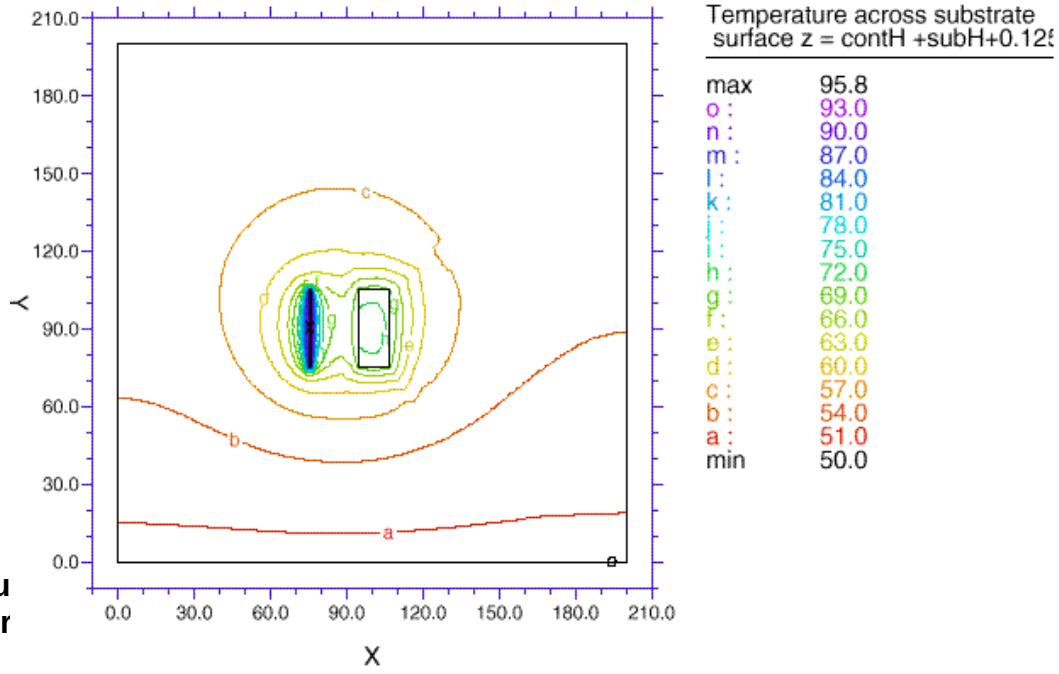


Figure 4.2.5 Original device.



Figu **al**
inter

4.3 Evaluation of the target circuit

Where are the effects of temperature distribution on the chip specially pertinent? Some typical application areas include:
Hot technologies - Technologies like GaAs FET, HBT, BJT and BiCMOS, contrarily to CMOS, dissipate significant power even in steady state. Several recent technologies including submicron CMOS technologies push the devices to run at high current to achieve better speeds and thermal effects thus become even more pronounced. For these technologies, the temperature variations between devices on the same die become important.
Matched devices - The correct behavior of designs relying on closely matched devices may be perturbed if temperature effects are not taken into account. The presence of a heat source next to theoretically matched devices will alter their parameters and may potentially disturb matching. As a consequence, the overall performance of the circuit may be upset. Circuits most sensitive to this type of effects are: differential circuits, current mirrors, matched resistor networks, etc.
Circuits with power stages - This class of circuits is particularly jeopardized by the lack of an appropriate thermal design loop. The presence of a power stage (line driver, laser driver) in close proximity of other blocks often causes a temperature gradient that affects a large neighborhood. The worst situation occurs when power stages are asymmetrically placed close to matched devices.

The algorithm has been applied to a design of an operational amplifier fabricated in a 0.6um GaAs process. The algorithm has helped to predict the temperature distribution on a die and to correct amplifier offset, a steady state example is given.

One of the very important parameters of an ampli-op is its offset voltage. A small deviation of this value will decide whether a given circuit pass or fail the tests. The typical value of the offset for the state-of-art wideband operational amplifiers with a power stage (e.g. HFA1109 from Harris, OPA650 from Burr-Brown) is about ±1mV with a guaranteed maximum of ±5mV. The offset value for the designed amplifier simulated with constant temperature assumption stays within the same range. The addition of temperature induced effects has shifted this value by approximately 2mV, which corresponds to 40% of permitted deviation, Figure 4.3.1 and Figure 4.1.2.

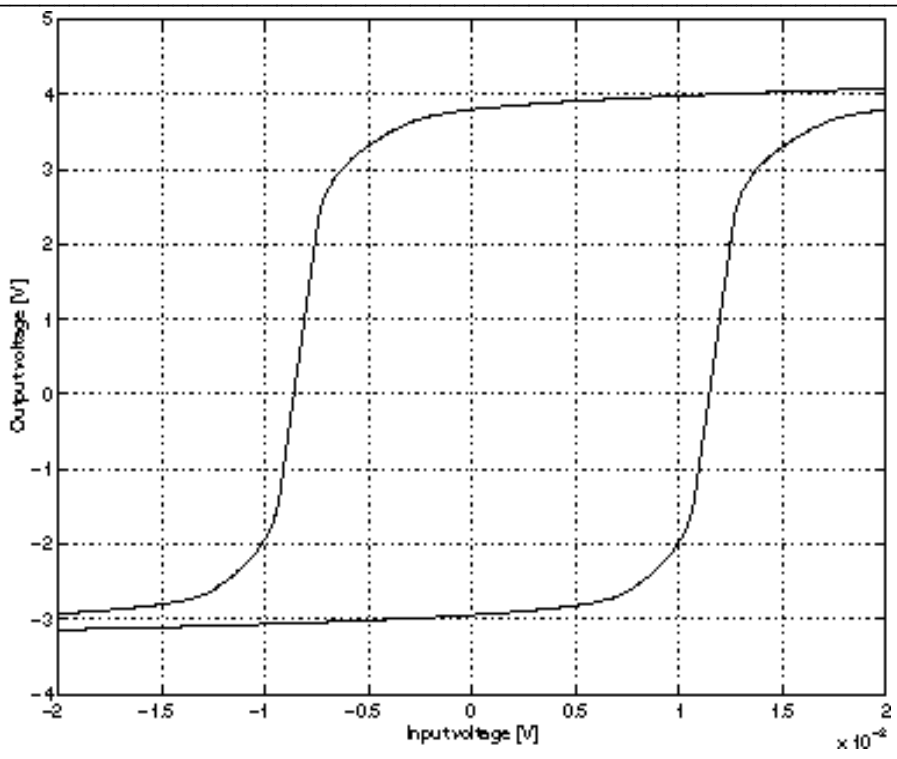


Figure 4.3.1 Variation of the offset of an operational amplifier due to the temperature distribution .

The presented TED software presents an advantage of a full integration within standard design flow, very fast algorithms to calculate thermal map, and a possibility to automatically compare the measured and simulated results.

4.4 Conclusions

A new methodology for thermal analysis fully integrated into design environment have been presented.

Compact thermal model were developed without increased element number in the circuit to be analyzed and allowing very fast thermal simulation times (1.5 s for a 1600 element circuit).

The presented results are validated against 3D FEM simulations and proved the accuracy and applicability of the presented methods and algorithms.

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